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Ge/GaAs HMT TECHNOLOGY BASED ON RPECVD

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<p>The following report details the progress on ONR contract number N-00014-86-C-0838 during the period from January 1, 1991 to December 31, 1991. This program is targeted at development of a Ge on GaAs High Mobility Transistor (HMT) technology. During this period, the work has focused on 2 areas. The first area described involves the effect of the Si deposition parameters on the electrical characteristics of the composite Ge-pseudomorphic Si-SiO₂ MIS structure. Complementary n and p type Ge MIS structures are presented which exhibit low midgap D_{it} values. The second area described involves the fabrication of Ge MISFET devices using the pseudomorphic Si-SiO₂ gate insulator. These n-channel transistors exhibit a transconductance of 24 mS/mm at a gate length of 2 microns.</p>					
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1.0 Introduction

The following report conveys the progress made during the annual period, from January 1, 1991 to December 31, 1991 for ONR contract number N00014-86-C-0838. Funding for the program is provided by the Strategic Defense Initiative under the Innovative Science and Technology through the Office of Naval Research. This program is a joint effort between the Research Triangle Institute's Center for Semiconductor Research and the North Carolina State University Physics department. The program is focussed on the development of Ge/GaAs high mobility transistor (HMT) technology. The program includes development of low temperature CVD deposition of SiGe alloy materials.

2.0 Low Temperature Ge Deposition on GaAs

Experiments have been carried out to investigate the effect of capping the backside of the GaAs substrate with nitride for Ge deposition. Even at 300 °C, the As partial pressure from GaAs is not negligible. The back side of the GaAs wafer has been uncoated for past experiments. Since the back side of the wafer does not get coated with Ge, the As vapor pressure from the backside of the wafer can be a source of n dopant throughout the Ge deposition run. The object of this experiment was to investigate the effect of the backside coating on the unintentional doping level in the material. The following experiments were carried out:

1. Deposition of Ge at 300 °C on uncoated GaAs at a rate of about 35

angstroms/min. (baseline run)

2. Deposition of Ge at 300° C on backside coated GaAs at a rate of about 17 angstroms/min.

3. Deposition of Ge at 300° C on backside coated GaAs at a rate of about 35 angstroms/min.

4. Deposition of Ge at 300° C on uncoated GaAs wafers sitting on a Si wafer as a backside proximity cap at rates of about 17 angstroms/min. and about 35 angstroms/min.

Resistivity measurement profiles and corresponding calculated doping profiles were made on each wafer to compare doping levels in the materials. The thickness of the layers was determined from the resistivity measurement profiles. The deposition rate was found to vary slightly between runs.

Figure 1 shows the doping profile for the baseline uncoated sample. The procedures used are sufficient to reduce the typical doping peak found at the interface between the GaAs and the Ge. However the overall doping level on the order of 10^{17}cm^{-3} . This sample was deposited at a relatively high deposition rate of 35 angstroms per minute. As expected the doping level is about a factor of 2 lower than that of films deposited at lower deposition rates.

Figure 2 shows the doping profile from a layer grown on a GaAs wafer which had its backside coated by Si_3N_4 . This layer was deposited at a rate of

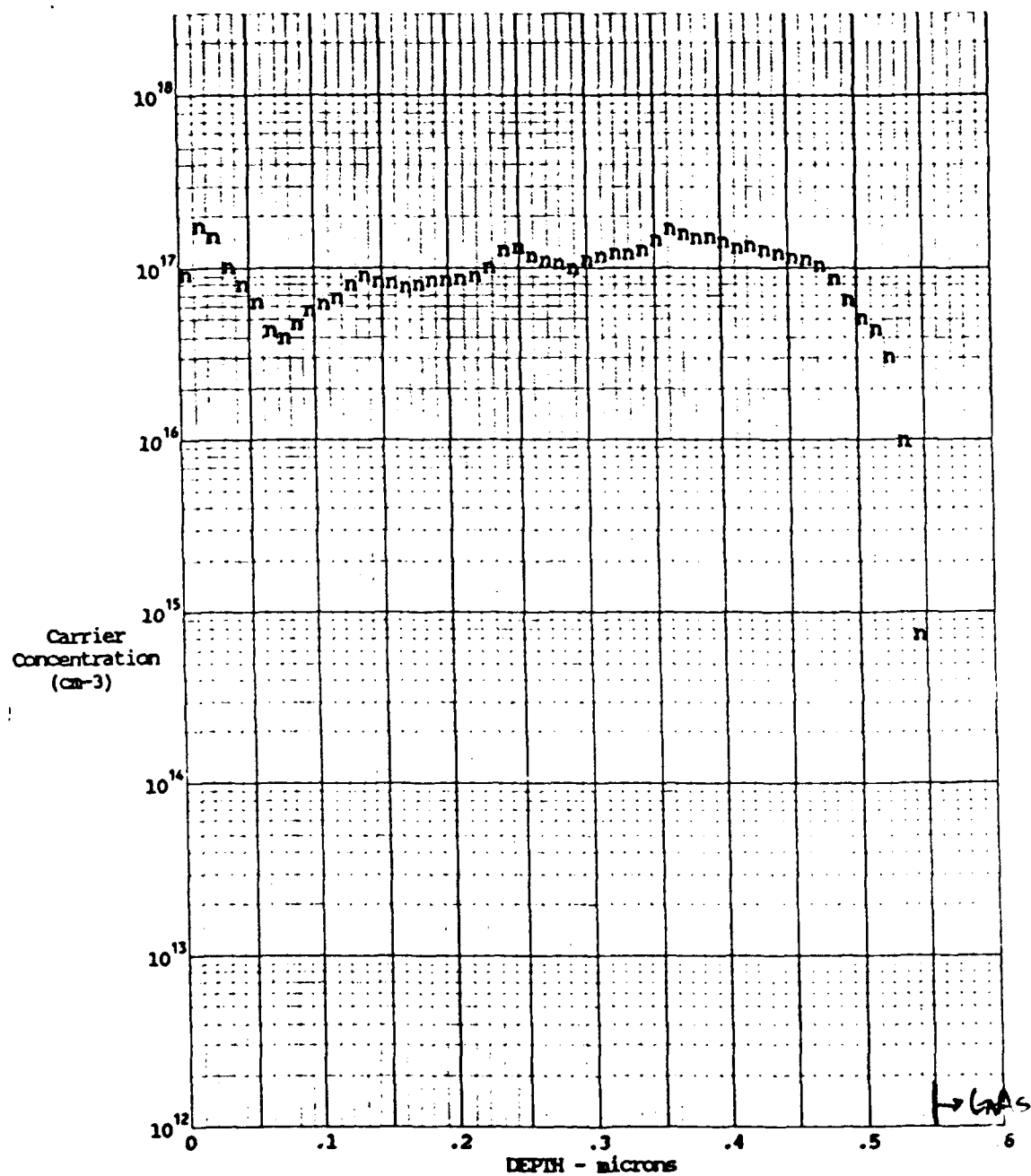


Figure 1 Doping profile for baseline Ge layer grown on uncoated GaAs.

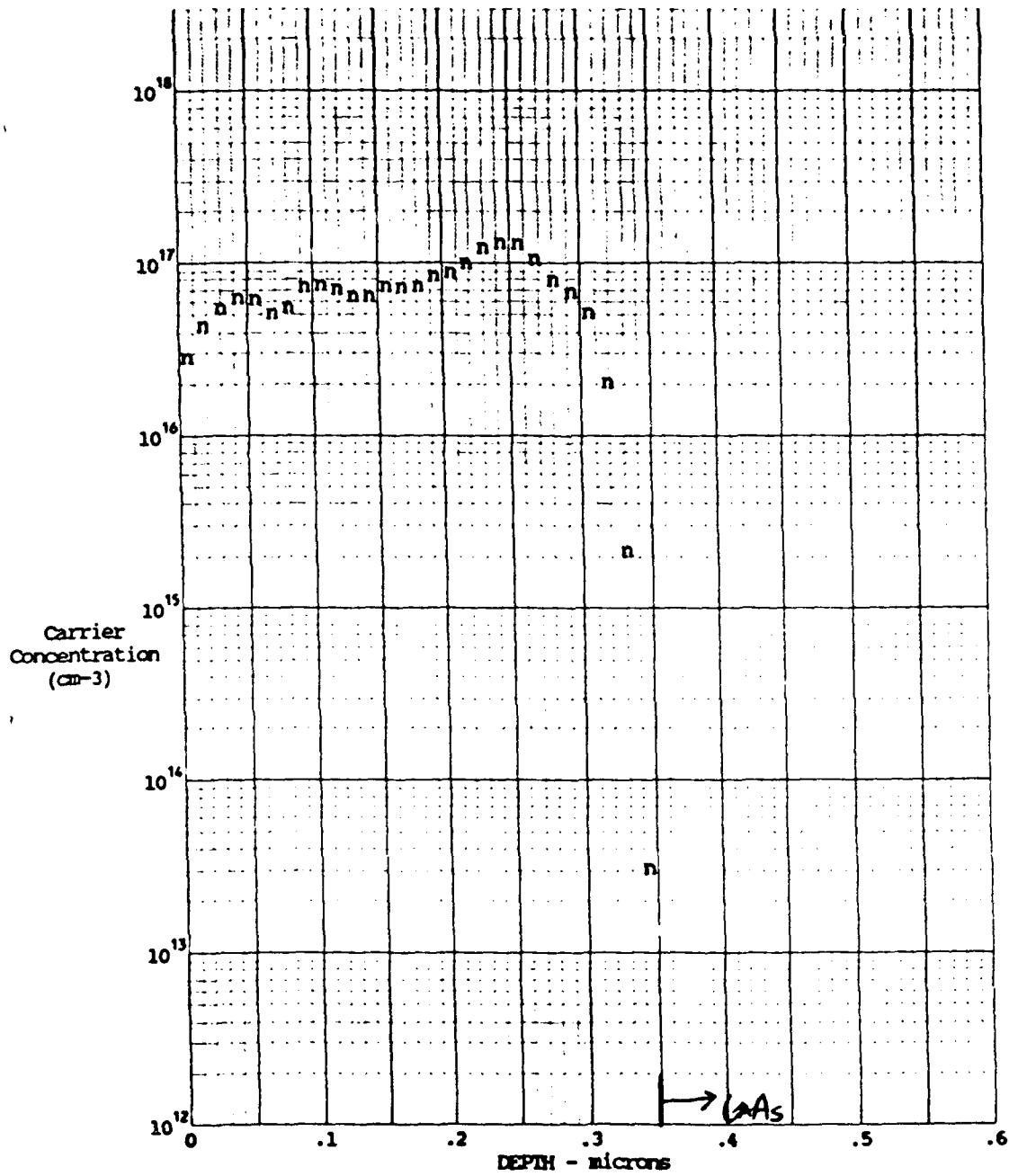


Figure 2 Doping profile from a Ge layer grown on a GaAs wafer which had its backside coated by Si₃N₄.

17 angstroms per minute. The doping level for this layer is, on the average, slightly lower than for the baseline layer. The purge after the in situ clean was only 15 minutes compared to a 20 minute purge for the baseline sample. This curtailed purge cycle may be responsible for the slight rise in doping found at the Ge GaAs interface. It is surmised that residual hydrogen in the chamber may be responsible for removal of As from the GaAs wafer during the initiation of the deposition process.

Figure 3 shows the doping profile from a layer grown on a GaAs wafer which also had its backside coated by Si_3N_4 . This layer was however grown at a rate of 33 angstroms per minute. This sample exhibits an average doping level which is over an order of magnitude lower than that of the baseline sample. Again there is a slightly higher doping level at the interface, but in this case the high level is in the mid 10^{16}cm^{-3} range. By combining the backside coating and the higher deposition rate it appears to be possible to achieve very low doping levels in the Ge or GaAs with very little interfacial spiking of the interfacial doping level.

Figures 4 (low growth rate 14 angstroms per minute) and 5 (high growth rate 34 angstroms per minute) show doping profiles from layers grown on uncapped GaAs wafers placed on a Si wafer as a proximity cap. In both cases a large doping spike was observed near the Ge GaAs interface. It is surmised that the space between the Si and GaAs wafer serves as a reservoir for hydrogen which is very difficult to pump out. In addition these runs had curtailed

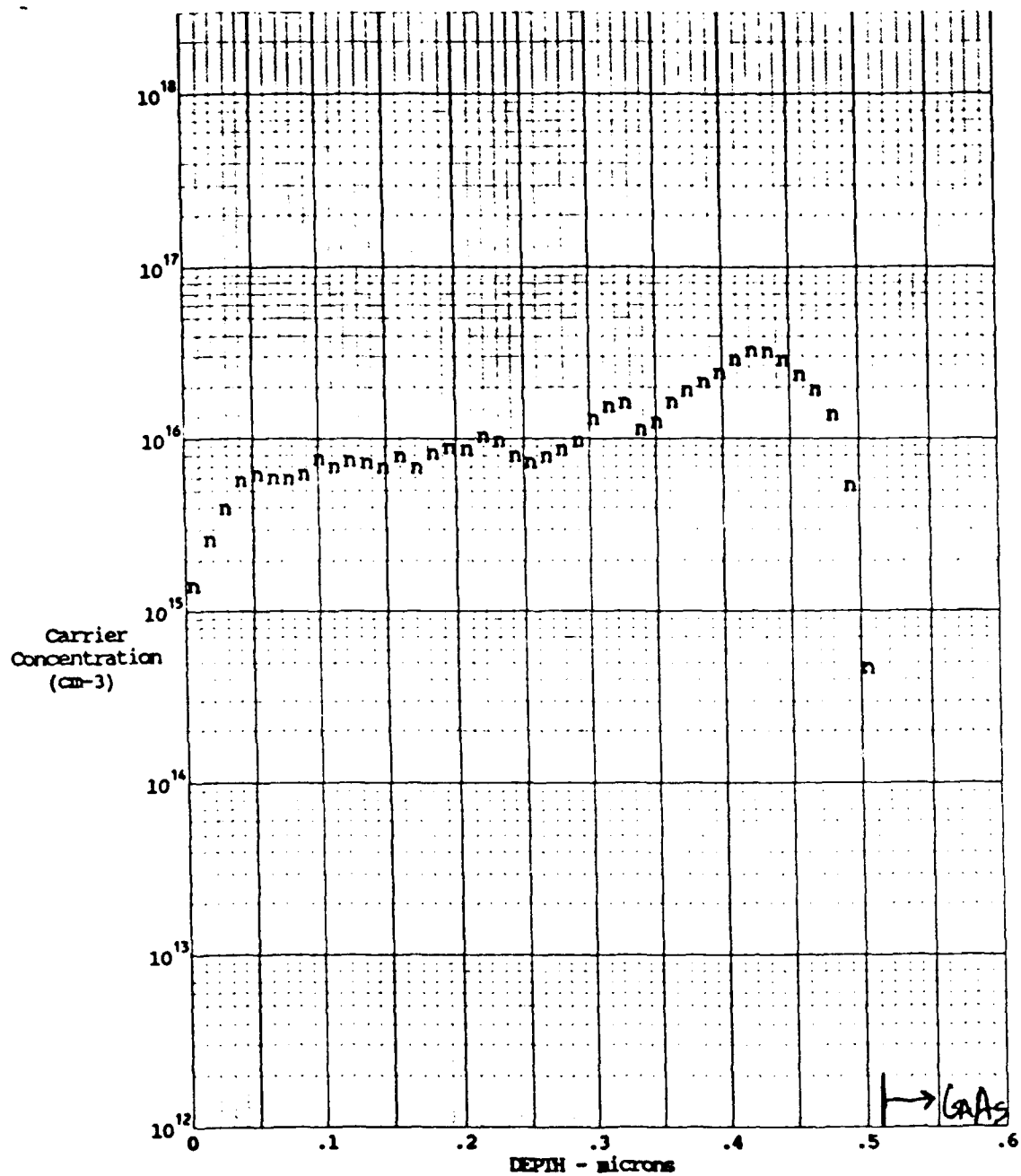


Figure 3 Doping profile from a Ge layer grown on coated GaAs at a high growth rate (33 angstroms per second).

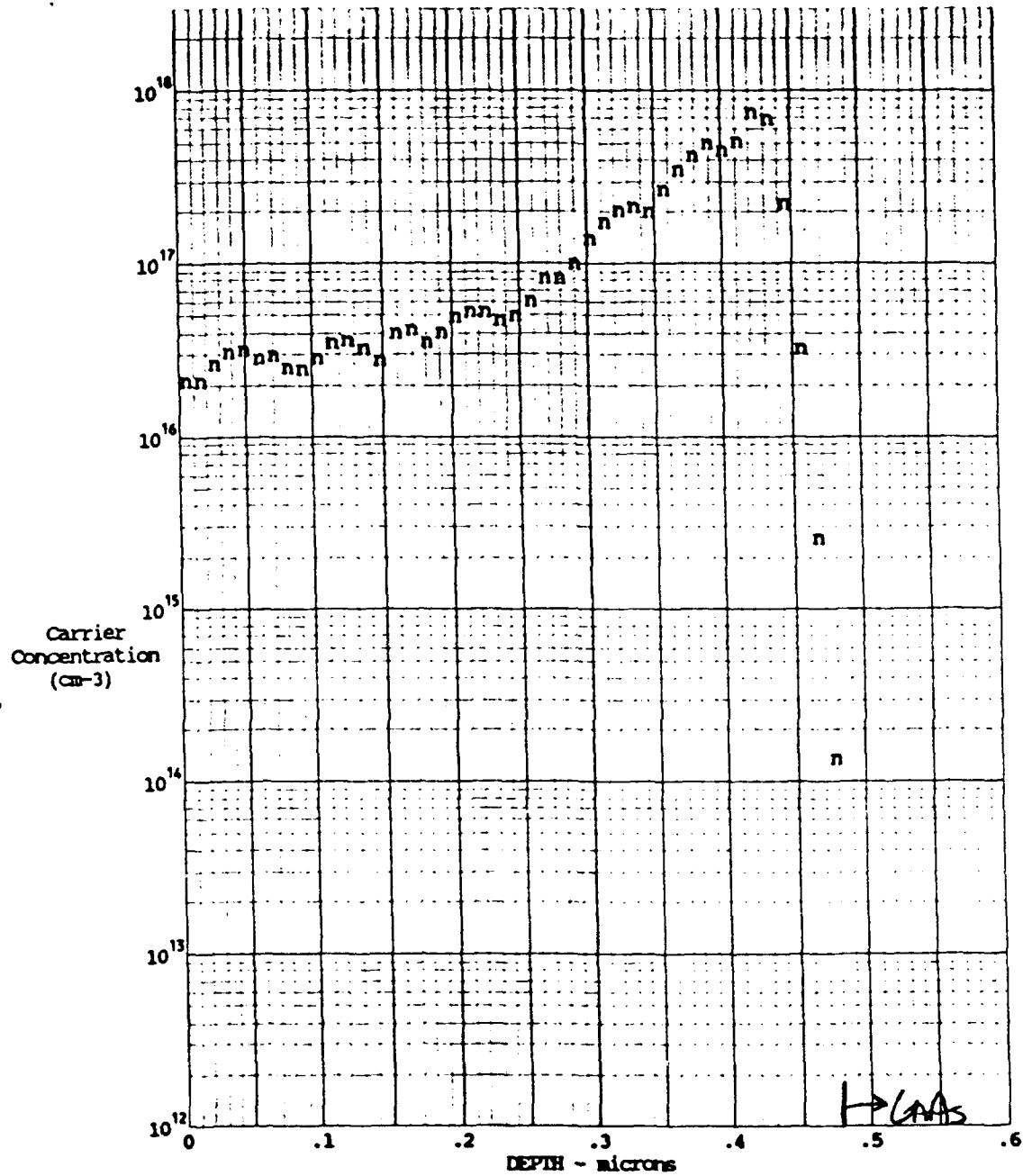


Figure 4 Doping profile from a Ge layer grown on uncoated GaAs with a Si wafer used as a backside proximity cap using a low growth rate.

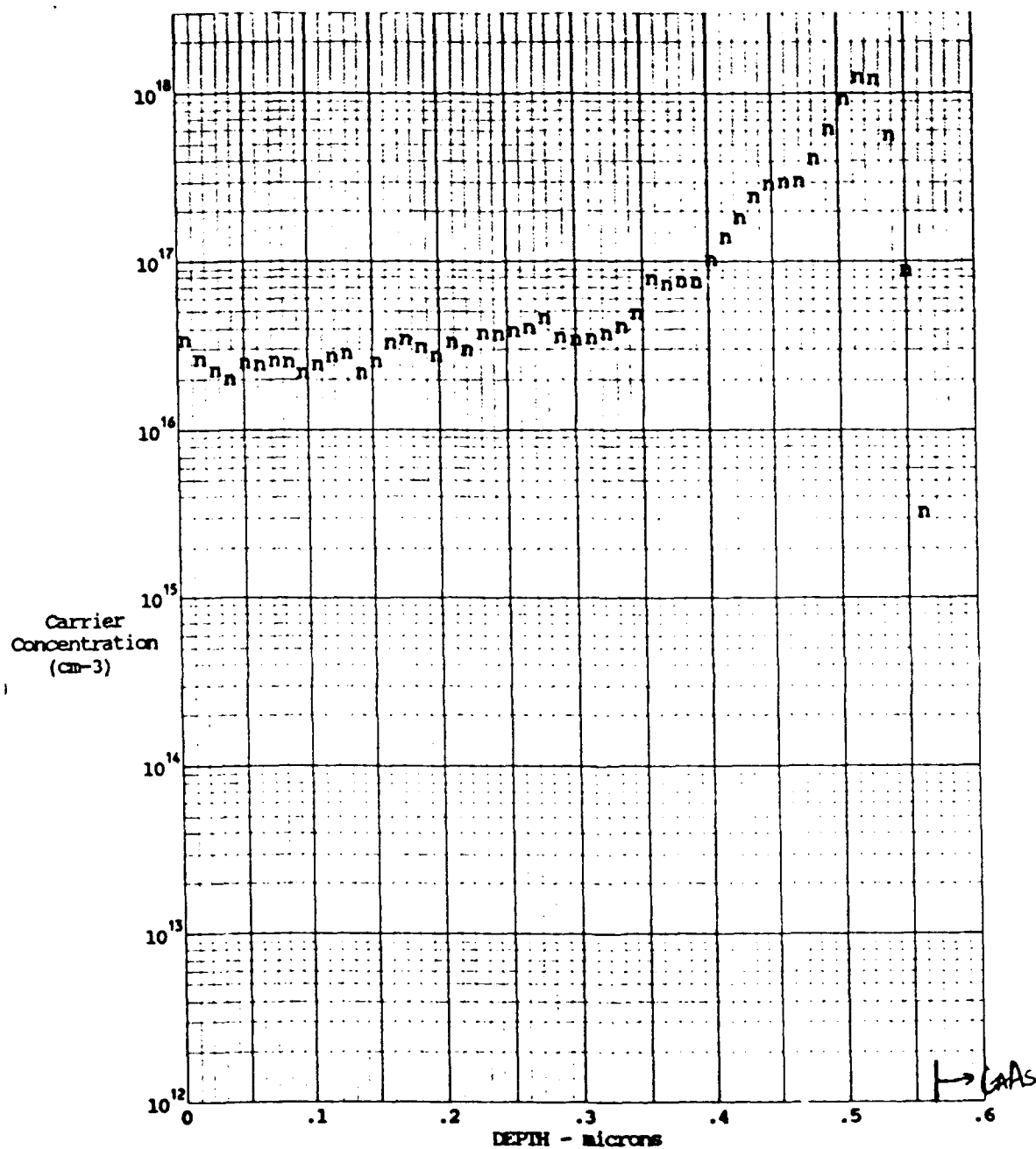


Figure 5 Doping profile from a Ge layer grown on uncoated GaAs with a Si wafer used as a backside proximity cap using a high growth rate.

purging cycles after the in situ clean process. None the less, the Si wafer seem to be somewhat effective at capping the backside of the wafer since the minimum doping in the 2 to $3 \times 10^{16} \text{cm}^{-3}$ was observed in both cases. These effect of the high deposition rate is not apparent between these two runs.

The major results of this experiment are as follows:

1. Backside capping of the GaAs wafer is useful for reducing the background doping in the Ge material deposited at 300° C.
2. Higher deposition rates accomplished by using higher GeH_4 flow rates lead to lower background dopant incorporation.

Residual hydrogen in the chamber likely leads to increased doping at the Ge GaAs interface. Adequate purging of the system after the in situ clean can greatly reduce this phenomenon.

3.0 Carrier Confinement in SiO₂/Si/Ge Heterostructure Inversion Mode MISFETs

Germanium MISFET device results are reported utilizing a SiO₂-crystalline Si heterostructure insulator on the Ge surface. Capacitance voltage measurements and transistor characteristics have revealed information on carrier confinement in n-channel and p-channel structures. Experiments have verified that the Si interlayer is in place and is not completely consumed by oxidation during processing. Electrical measurements indicate that electrons can enter the Si layer with only a small barrier, however, holes are confined in the Ge material across the operating gate bias range. In addition, immobile charge at the Si/Ge interface causes the mobile holes to be confined approximately 2 nm away from the surface of the Ge. Room temperature and low temperature MISFET characteristics show that p-channel performance is enhanced at low temperature, but n-channel performance is severely degraded at low temperature. This observation is consistent with the carrier confinement observations. The p-channel devices exhibit room temperature peak effective mobilities of up to 429 cm²/V-sec with a transconductance of 51 mS/mm at a gate length of 2 microns.

3.1 Background on Device Structures

In the technology of heterostructure devices, carrier confinement by heterojunction barriers is of critical importance. Recently, a good deal of attention has been focused on heterostructure field effect transistors formed using the Si-Ge materials system [1,2,3], and in particular, on the physics of charge

confinement in these devices. We report an investigation of inversion layer confinement in the Ge portion of a Ge/Si-SiO₂ heterostructure/MIS device. The Ge MIS device utilizes an ultra-thin, crystalline Si interlayer (~ 20 Å) to form an electrical interface with the SiO₂ insulator[4]. The Si layer precludes the formation of the detrimental Ge-oxides at the interface and forms an excellent interface with the overlying SiO₂[5].

3.2 Device Fabrication and Testing

The MISFET devices were fabricated in the following manner. Ge wafers obtained from Eagle Pitcher Incorporated and Metal Hoboken Overpelt were selectively implanted for source drain formation. N-channel devices were fabricated on p type (100) wafers implanted with phosphorus. P-channel devices were fabricated on n type (100) wafers implanted with boron. After implantation and stripping of the implant mask, the wafer was wet chemically cleaned immersing the wafer for 1 minute in NH₄OH (1) : H₂O₂ (2) : H₂O (1600) solution followed by immersing for 1 minute in NH₄OH (1) : H₂O (15). The wafer was then loaded into the remote plasma enhanced CVD reactor for processing. This reactor, the in situ cleaning process, and deposition processes have been described in detail elsewhere [4,6]. The wafer received a 20 second in situ activated hydrogen clean. Next, 15 to 20 angstroms of Si was deposited on the wafer followed by deposition of 150 to 200 angstroms of SiO₂. The cleaning and deposition processes were performed at 300 °C. To test whether the Si layer remained in tact after the SiO₂ deposition, the oxide layer was etched away in

dilute HF and the test sample was analyzed with Xray photoemission spectroscopy. The Si layer was seen to be intact on the Ge surface. After insulator deposition the sample was metalized with aluminum for gate formation. The sample received a 30 minute 400° C post-metallization anneal in nitrogen. This anneal together with the 300° C processes was adequate to activate the implanted species. The gates were patterned by etching. The ohmic contact pattern was applied, windows were opened using buffer HF etching, and the non-annealed aluminum contacts were formed by liftoff. The devices were tested at this point. MIS capacitors, MISFETs and transmission line model contact resistance patterns were included on the test die.

The MIS capacitor structures were tested at 1 MHz and low frequency (quasi static). The characteristics of the n-channel and p-channel samples are shown in Figures 6 and 7 respectively. The midgap interface state densities calculated from this data was noted to be in the mid $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ range for both n and p channel devices at room temperature. Note that the maximum capacitance in accumulation and inversion is different in both n-channel and p-channel cases. The data indicates that the electrons are allowed to enter the Si material at the interface thus leading to a higher capacitance in inversion for the n-channel device, and accumulation for the p-channel device. If it is assumed that the difference in the quasistatic and 1 MHz accumulation capacitance in the p-channel case (Figure 7) is indicative of trapping of the electrons in the Si layer, then the difference in these capacitances can be used to estimate

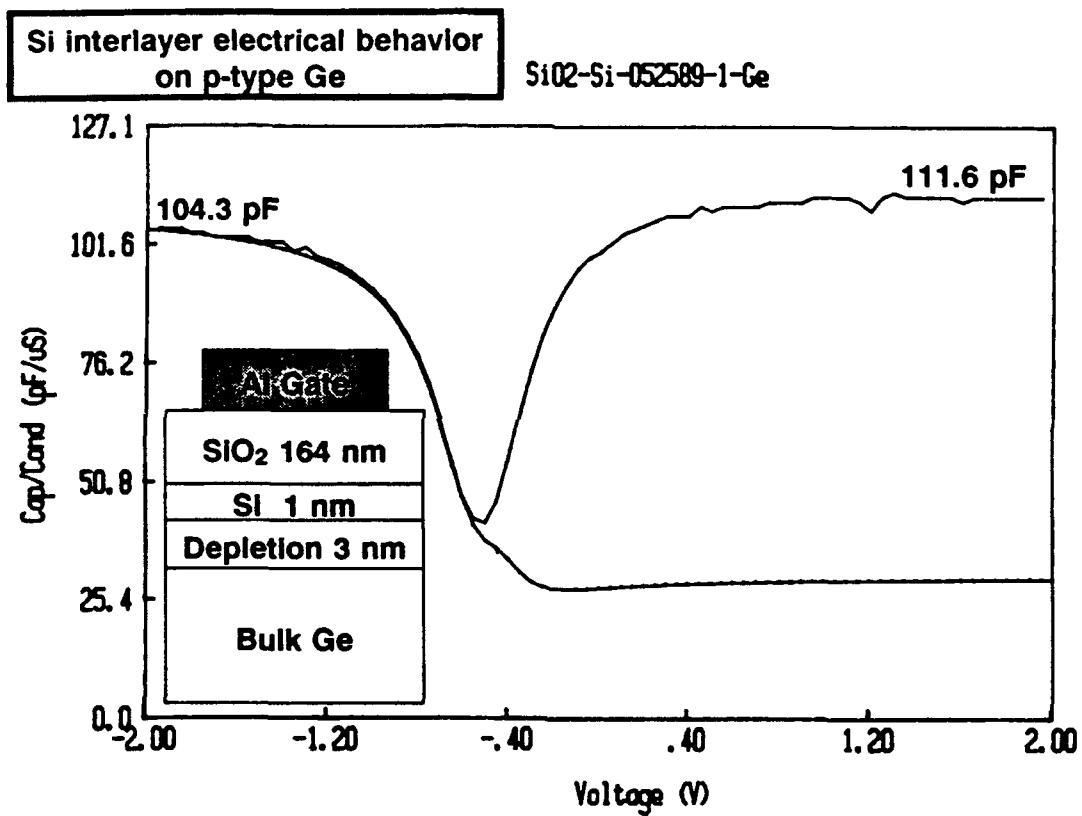


Figure 6 CV characteristics of an MIS capacitor on p-type Ge (n-channel).

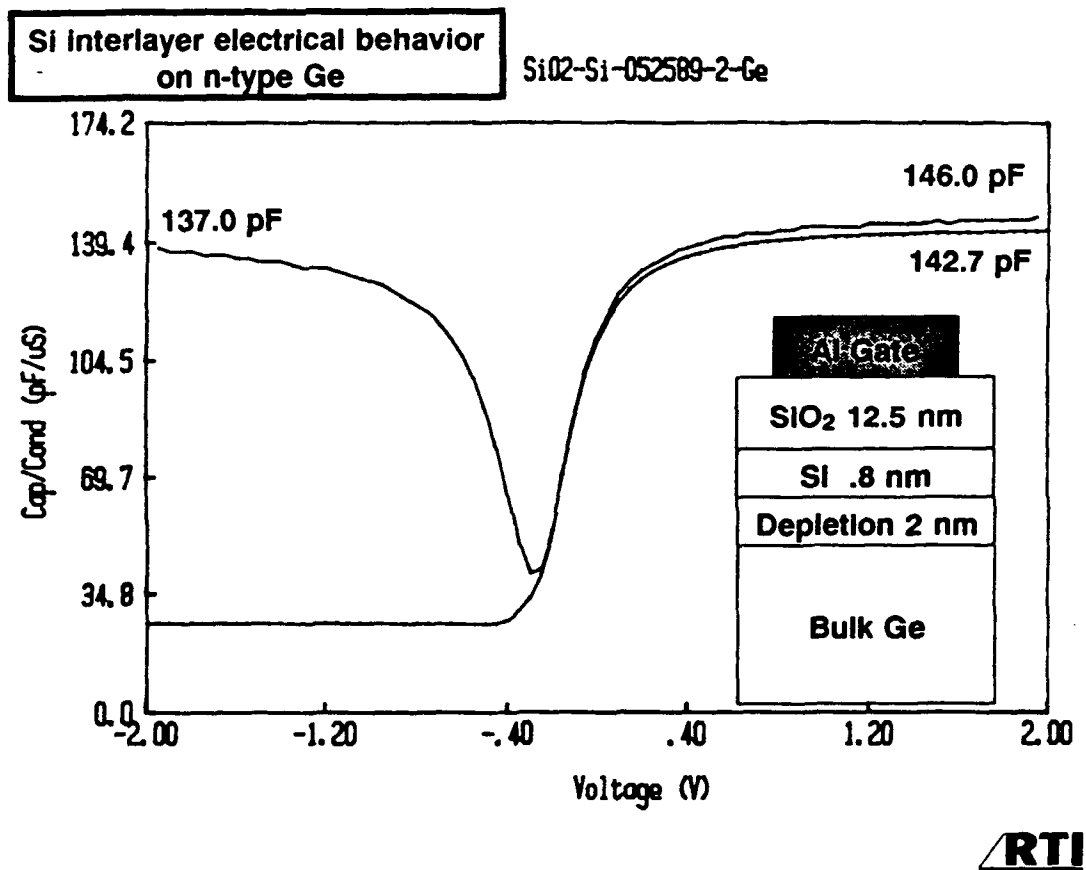


Figure 7 CV characteristics of an MIS capacitor on n-type Ge (p-channel).

the Si layer thickness. Conversely the holes are apparently not allowed to enter the Si layer. The maximum value of capacitance for the hole accumulation or inversion indicates that the holes are in fact held away from the Ge/Si interface electrostatically by some 20 angstroms over a wide bias range. Note that the high frequency and quasistatic hole accumulation capacitances are identical. 1 MHz capacitance voltage data was measured at 77K. This data is indicative of majority carrier behavior at low temperature. The curve for the p-type material was shifted in voltage slightly, however the curve for the n-type material was severely stretched out. These measurements indicate that there is little hole trapping in the structure but there is a high density of electron trapping.

The n and p-channel MISFET characteristics are shown in Figure 8. The room temperature mobilities of the devices appear to be similar, although the transconductance of the p-channel device is somewhat higher than that of the n-channel device. At 77 K the performance of the n-channel device is degraded by a factor of approximately 100, while the performance of the p-channel device is enhanced by approximately a factor of 2.

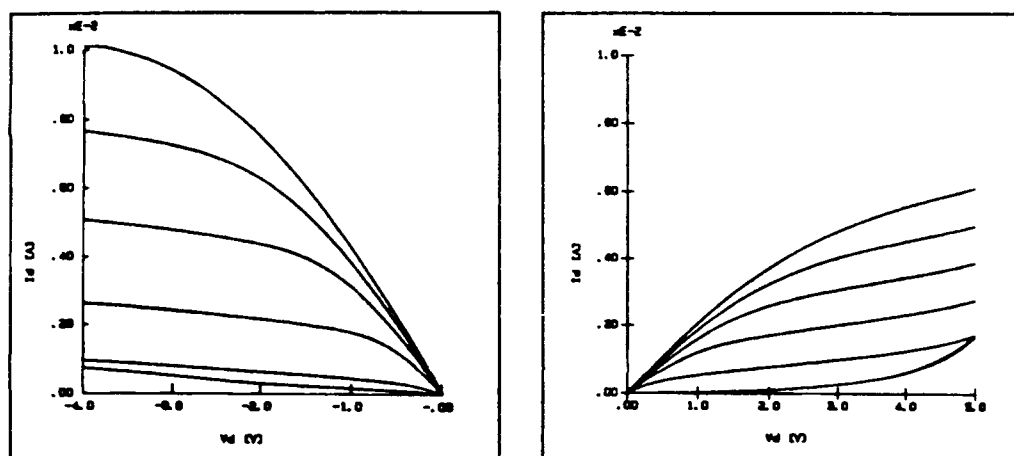
The p-channel device shown in Figure 8 was fabricated using MHO "zero etch pit density" material exhibited room temperature transconductances as high as 51 mS/mm with a peak effective hole mobility of $430 \text{ cm}^2/\text{V}\cdot\text{sec}$ at a gate length of 2 microns. This device performance is comparable to n channel Si MOSFET performance.

The origin of the hole barrier at the Si/Ge interface is not completely clear at this point. It is likely that a large portion of the barrier is due to the valence band discontinuity, as pointed out by Garone et al [1]. However, Milnes and Feucht point out that interface states or dislocation states can dramatically change the effective barrier at a heterojunction [7]. In the case presented here, donor like states which are positively charged when empty could explain the electron trapping behavior, and could as well account for the high hole barrier that exists at the Si/Ge interface.

3.3 Conclusions

Heterostructure Ge/Si/SiO₂ devices have been demonstrated. Electrical test data indicates that holes are confined in the Ge material away from the Si/Ge interface and in fact appear to form a buried channel layer. Electrons are not confined in the Ge and appear to become trapped in the Si layer. The p-channel devices show much promise for high performance p-MOS transistors with characteristics similar to those of Si n-MOS transistor of comparable geometry.

Demonstration of p and n Channel Inversion Mode Ge MOSFETs



- p channel inversion mode MOSFET
- Lg 2 microns Wg 50 microns
- $G_m = 51 \text{ mS/mm}$
- Peak Effective Mobility $429 \text{ cm}^2/\text{Vsec}$

- n channel inversion mode MOSFET
- Lg 2 microns Wg 50 microns
- $G_m = 22 \text{ mS/mm}$
- Peak Effective Mobility $440 \text{ cm}^2/\text{Vsec}$

Figure 8 p-Channel and n-Channel Ge MOSFET characteristics

4.0 SiGe Epitaxial Deposition at Low Temperature

Studies have been carried out to investigate the effects of plasma power and deposition temperature on SiGe films deposited by remote plasma enhanced chemical vapor deposition. This study includes determination of Ge mole fraction vs. silane to germane flow ratio, analysis of surface morphology as well as unintentional carrier density and n-P junction behavior. For all deposition it was assumed that low base pressure in the RPECVD reactor was necessary for high quality epitaxial deposition. The base pressure achieved prior to beginning a run was typically 1×10^{-8} torr or lower.

4.1 SiGe Composition

The RPECVD process for depositing SiGe material utilizes silane and germane gases as the source gases for the deposition. The composition of the alloy material can be controlled by the ratio of silane to germane used. Samples were grown at various ratios, and the compositions were checked using RBS. Figure 9 shows a plot of the results of this study. For silane to germane ratios ranging from 2 to 8 the composition varied from 50% Ge to about 25% Ge.

4.2 Surface Morphology

Smooth surface morphology is an essential attribute of semiconducting materials used in IC fabrication. It was found that both the deposition temperature and the plasma power affect the surface morphology. The major surface defects noted by SEM inspection were small hillocks. The density of these

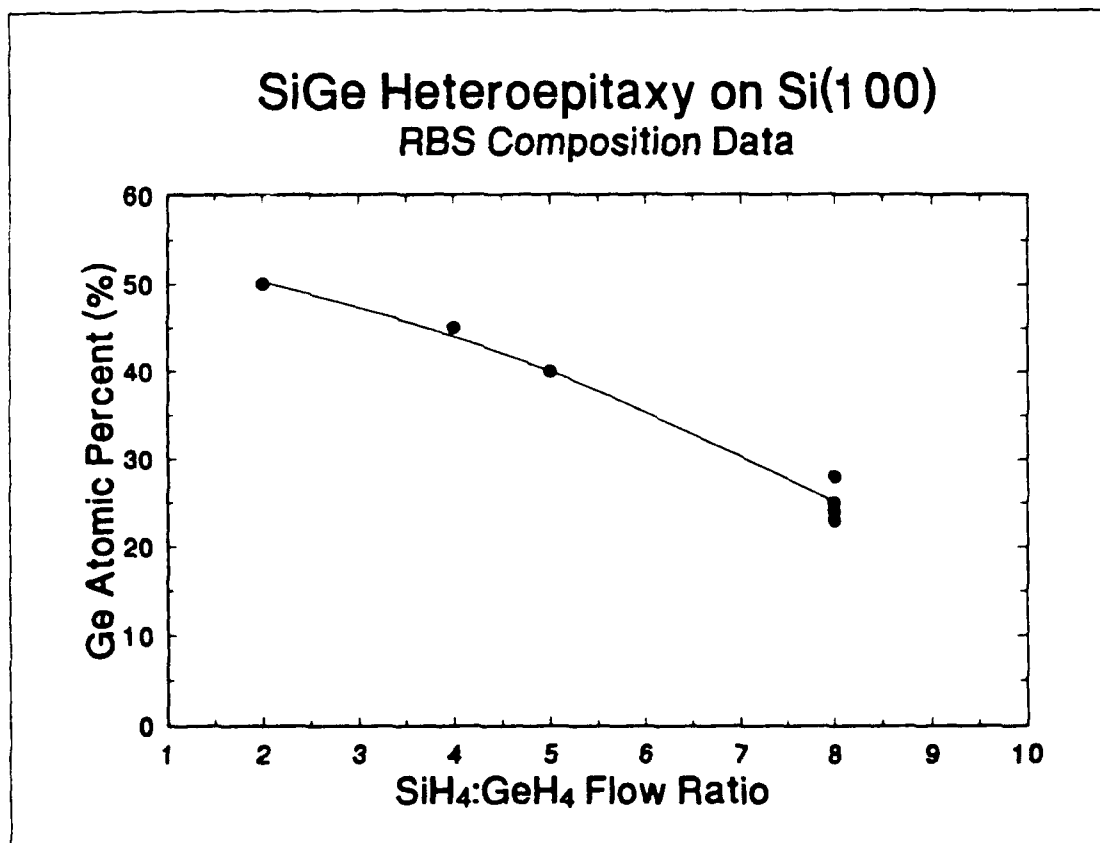


Figure 9 SiGe alloy composition vs. silane to germane flow ratio.

hillocks could be varied by changing the deposition conditions.

The deposition temperature had a dramatic effect on the density of the hillocks. The hillock density was dramatically reduced by raising the deposition temperature from 300° C to 400° C. It was noted that for Ge films, if the temperature was raised above 400° C, islanding of the Ge during growth was noted. This islanding ultimately leads to rough surface morphology.

The deposition power also had a noticeable effect on the hillock density. At lower powers the hillock density was higher than at high powers. The reason for this decrease with power is not apparent and is the subject of further investigation.

4.3 Electrical Characterization

Films were characterized electrically using Hall measurements and n-P (SiGe-Si) heterojunction characteristics. A temperature of 400° C was chosen for this work because morphology studies indicated that this was a reasonable low temperature to work at. The silane to germane ratio used was 8 to 1 giving a Ge composition of about 25%. The effect of plasma power variation on electrical performance was examined.

Figure 10 shows the effect of plasma power on the unintentional doping level of the material. The doping is n type. At 10 watts the carrier density is in the mid 10^{16}cm^{-3} range. At 30 watts and above the carrier density levels off in the mid 10^{17}cm^{-3} range. The indications are that the unintentional n type

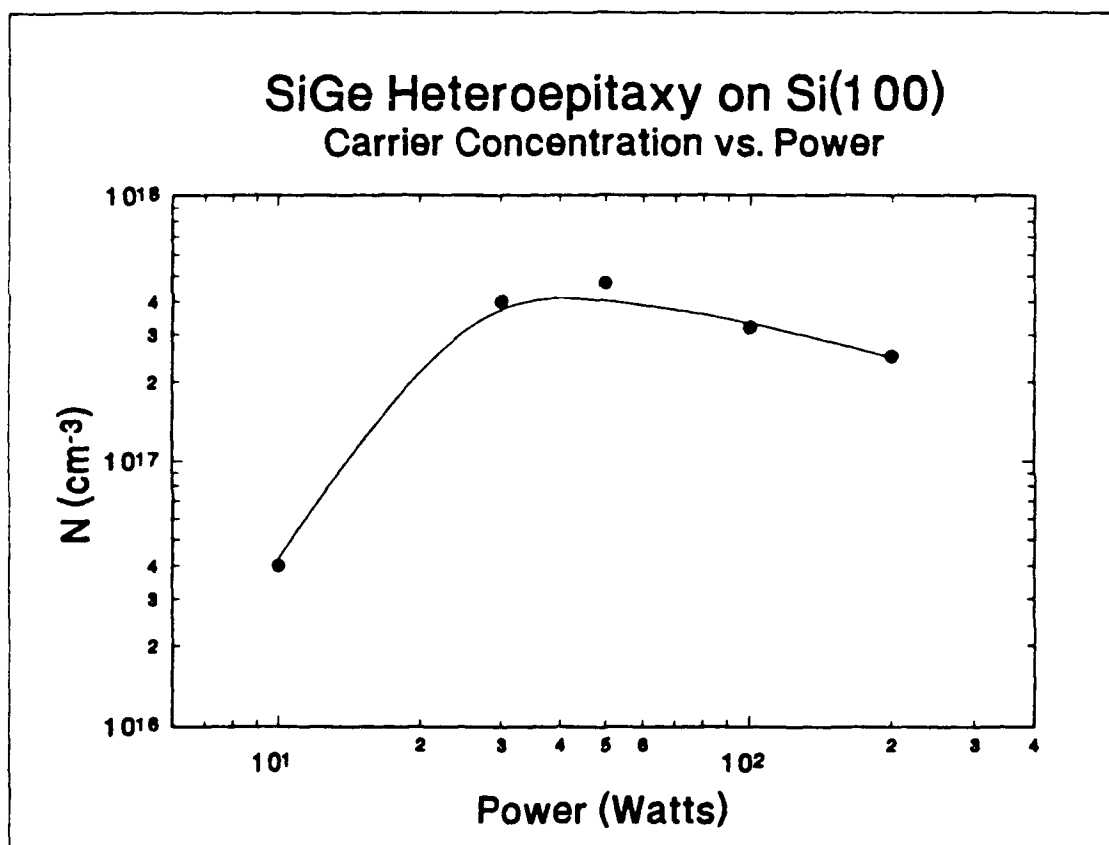


Figure 10 The effect of plasma power on the unintentional doping level in the material. The doping type is n.

doping is likely coming from slight erosion of the RHEED phosphor screen. The screen is covered by a shutter but the shutter is by no means gas tight. We have noted higher doping levels in the case where the screen was left unshuttered as opposed to the cases where the screen was covered by the shutter. The Hall mobility does not seem to be a particularly strong function of the the plasma power as shown in Figure 11.

The heterojunction reverse leakage behavior shows only weak trend toward higher leakage at higher power levels. Experiments indicate that the leakage current is a strong function of thickness. The power series done before utilized fairly thick layers of material. Thin layers on the order of 400 angstroms have shown superior n-P heterojunction behavior. Further study needs to be done comparing the effect of power on junctions fabricated using thin layers.

4.4 Phosphine doping SiGe Material using the Remote Plasma Process

Gas phase n-type doping of Si and SiGe films has been accomplished using phosphine as the doping source. The gas concentration used was 100 ppm phosphine in He. The dopant activation is very high in the plasma activated process. Low temperature pyrolytic processes have had difficulty activating high concentrations of n-type dopant without resorting to high temperature annealing cycles.

In a preliminary experiment with a low temperature Si layer, an activated level of $5 \times 10^{19} \text{cm}^{-3}$ has been measured. SIMS characterization of the sample

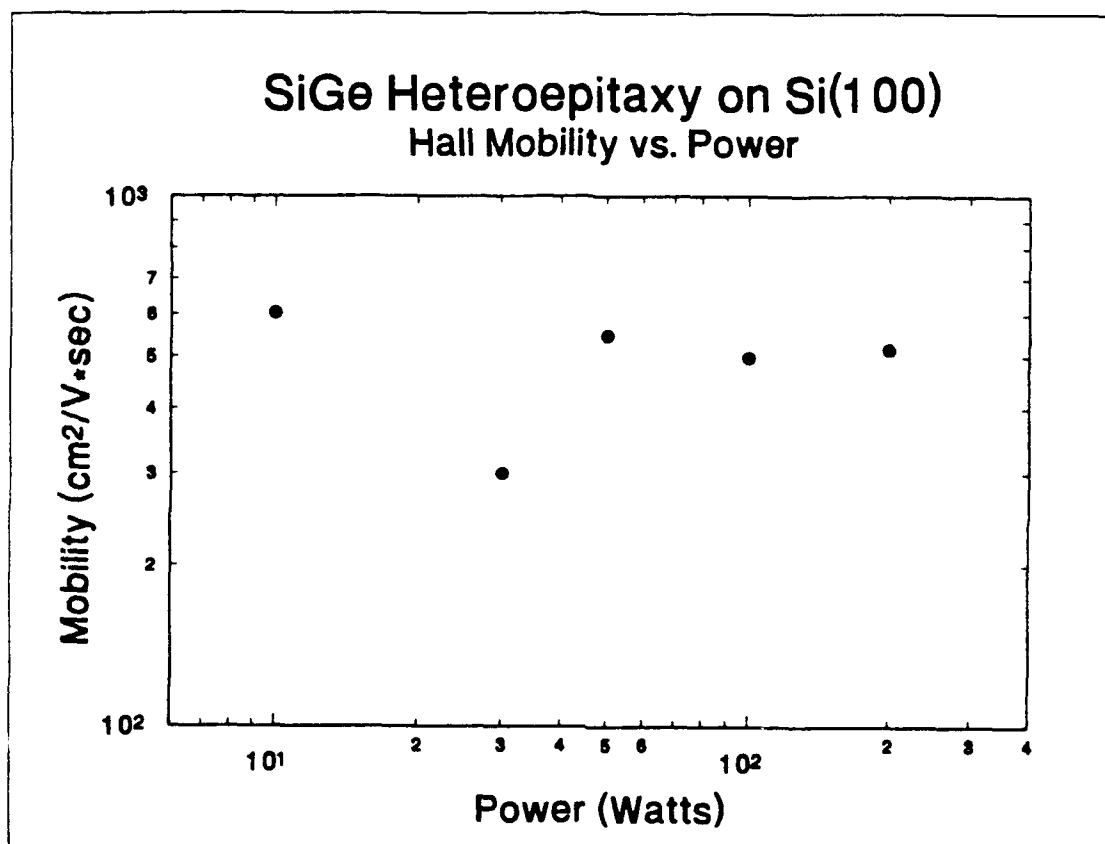


Figure 11 Hall mobility vs. plasma power. Values of mobility vs. carrier density are close to or above those for Si except in the 30 watt case.

indicates that the electrical activation is at least 50%. It is interesting that if hydrogen is incorporated in the growth environment as a diluent gas, the doping by phosphine is not seen. It is not clear whether the hydrogen removes the P from the layer or prevent electrical activation. SIMS is to be carried out on this sample to determine this issue.

The results of phosphine doping of the SiGe alloy layers are shown in Figure 12 and 13. Control of the doping level between the unintentional level in the mid 10^{17} and a doped level in the upper 10^{19} range. The doping level appears to saturate with phosphine flow above 20 sccm at $6 \times 10^{19} \text{cm}^{-3}$. Mobilities consistent with the doping level were measured. This is a phenomenally high n type doping level for a low temperature deposition process with no subsequent anneal.

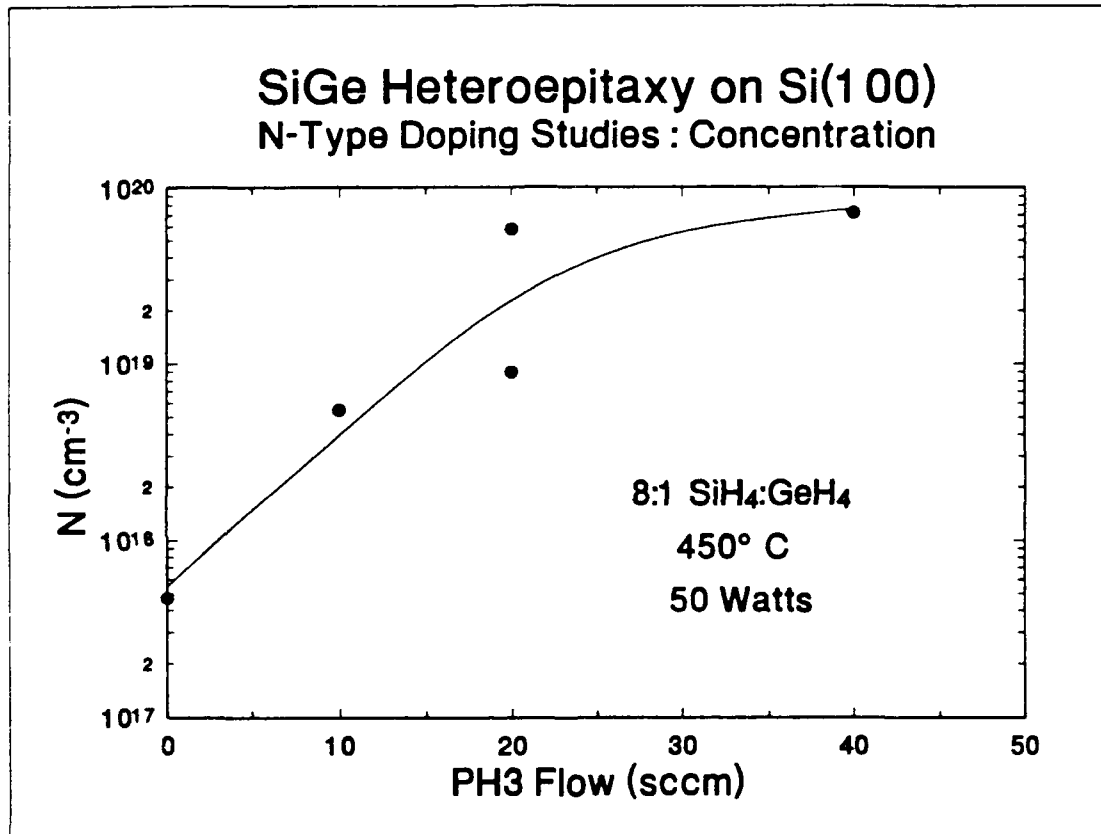


Figure 12 Carrier concentration vs. Phosphine flow rate.

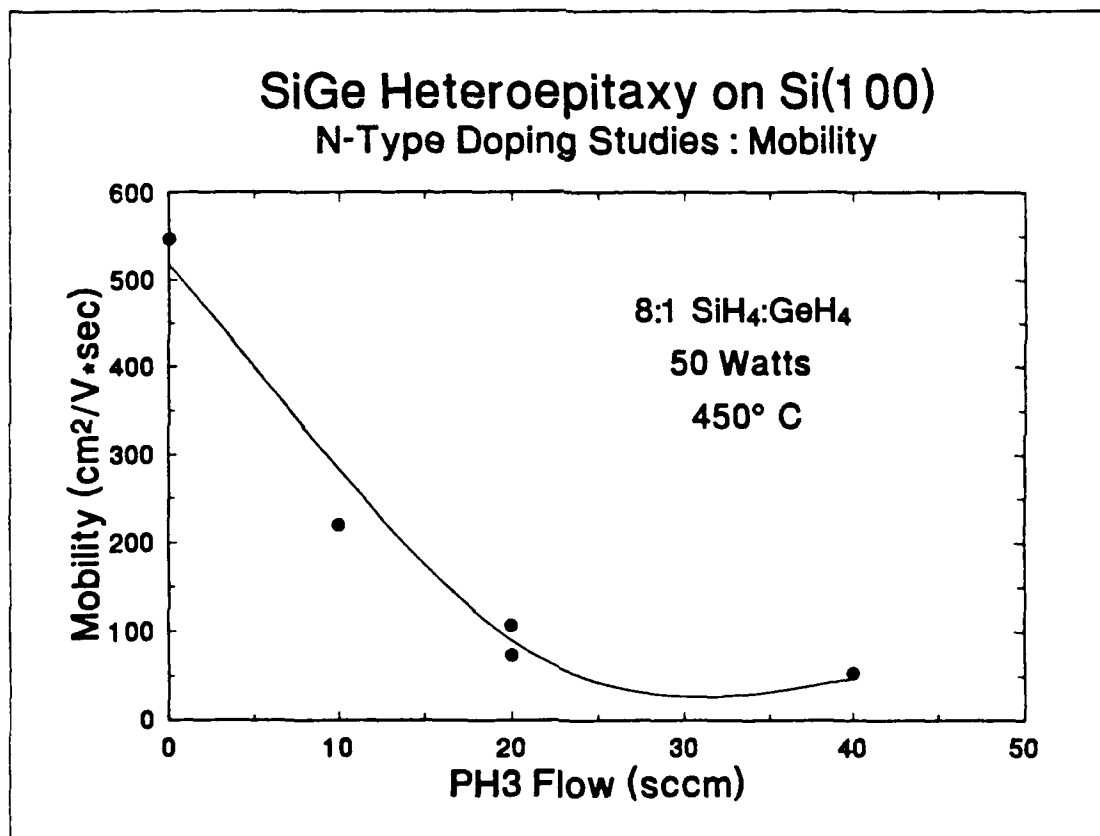


Figure 13 Carrier mobility vs. Phosphine flow rate.

5.0 Future Work

The proposed work for the next contract period involves fabrication of SiGe based devices and further development of the SiGe alloy deposition technique. As well a task to investigate deposition and characterization of dilute Si-C or SiGeC alloys has also been proposed. The epitaxial deposition system is being modified as shown in Figure 14 to vacuum integrate dielectric deposition and epitaxial deposition together in separate chambers. The epitaxial chamber is designed with no elastomer seals to provide a high purity system with as few virtual reservoirs for gas as possible. This system will allow fabrication of epi-dielectric system with maximum purity for the epi process and no air exposure between processes.

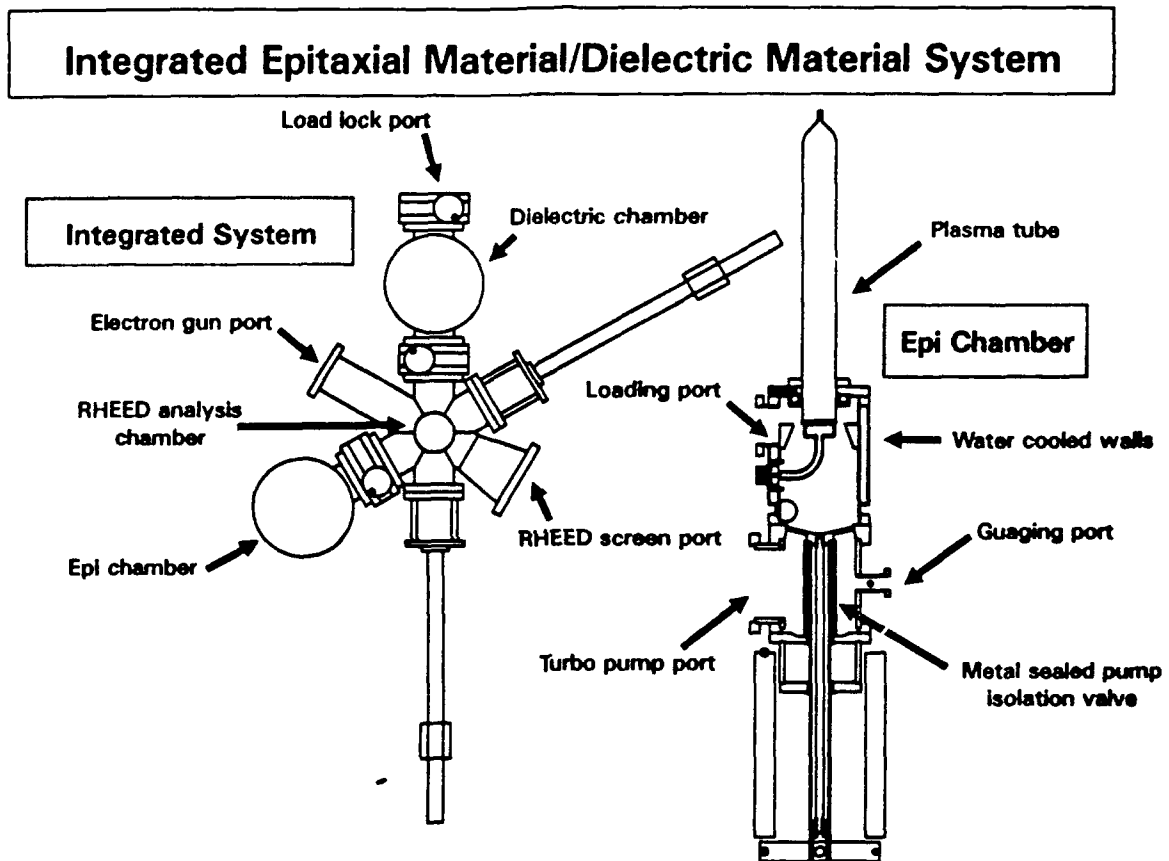


Figure 14 Modified RPECVD system integrating epitaxial deposition and dielectric deposition.

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